High Power Density Power Management IC Module with On-Chip Inductors

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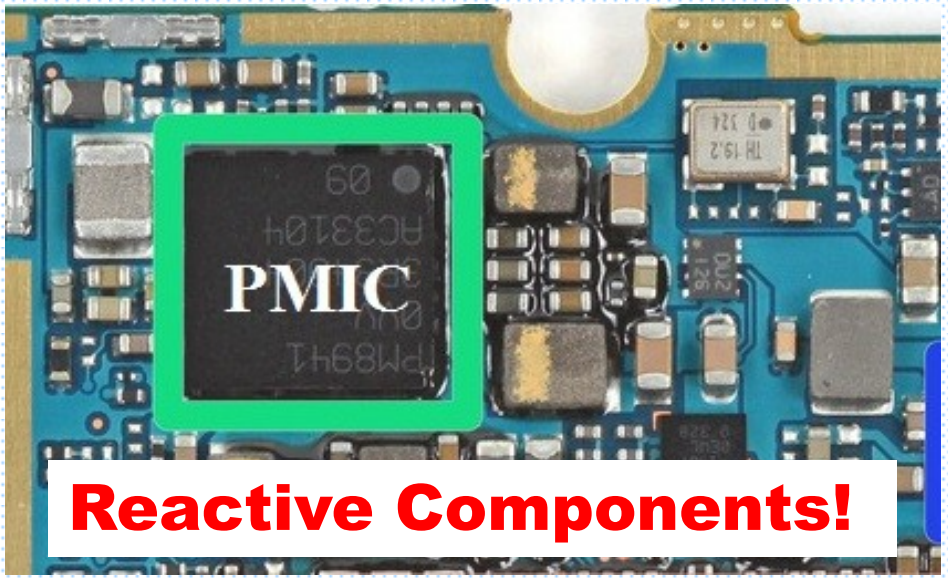
Presentation Outline

- Introduction and Motivation
  - Goal of the collaborative research
- High density power management architecture
  - Topology and principle of operation
  - Comparison with conventional architecture
- IC implementation with on-chip inductors
  - High density power management modules
  - Experimental Results
- Conclusions

Introduction and Motivation

- In a conventional power management solution for portable applications:
  - As many as 30+ separate dc-dc power supplies
  - Take up to 80% of overall device volume
  - Reactive components consume most of the volume

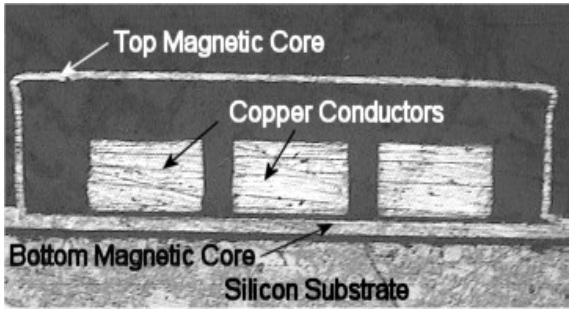


http://https://www.ifixit.com/Teardown/Nexus+5+Teardown/19016

Nexus 5 Smartphone

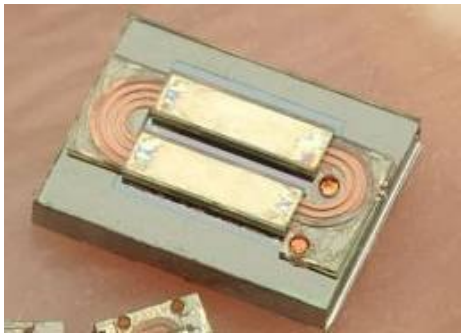
Tyndall Micro-fabricated Magnetics on Silicon

- Electroplated copper windings.
- Thin-film, electroplated magnetic core.
- Design optimization process
  - Focus on efficiency and footprint.
  - Coupled to validated models.



Cross section of a micro-inductor

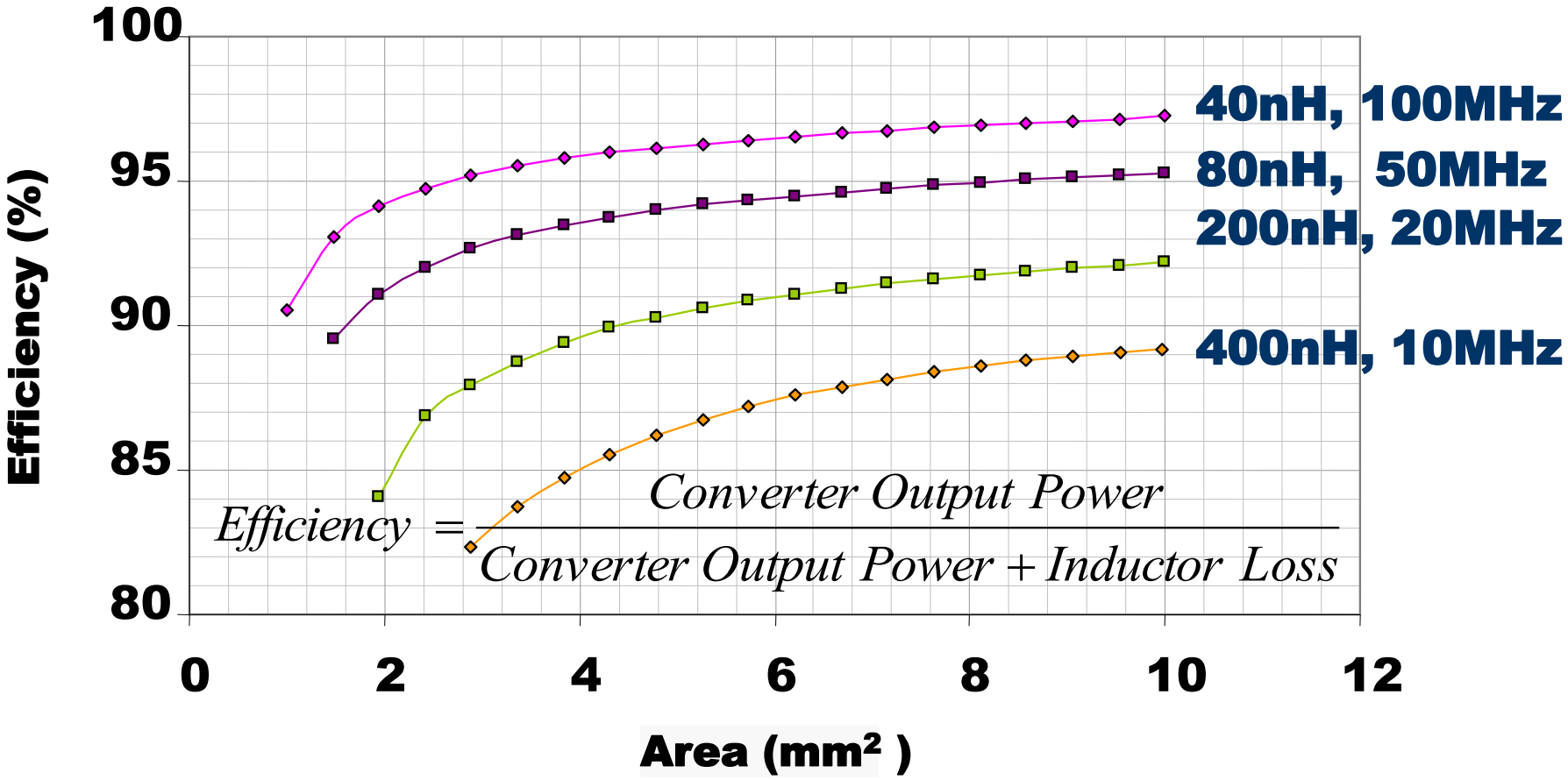
- Race-track shape to achieve:
  - good frequency response
  - high inductance density
  - Low DC resistance



- CMOS-compatible process:
  - Copper coils deposited by electroplating
  - Core consists of thin film of NiFe alloy deposited by electroplating

Micro-inductors fabricated on 4 inch Si wafer

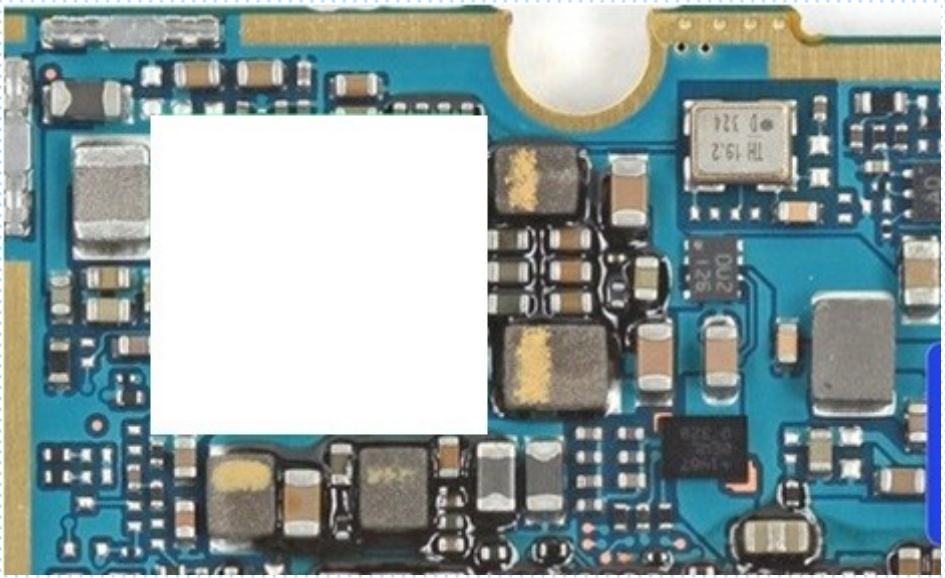
Micro-inductor efficiency increases with frequency multi-parameter optimization at 500mA

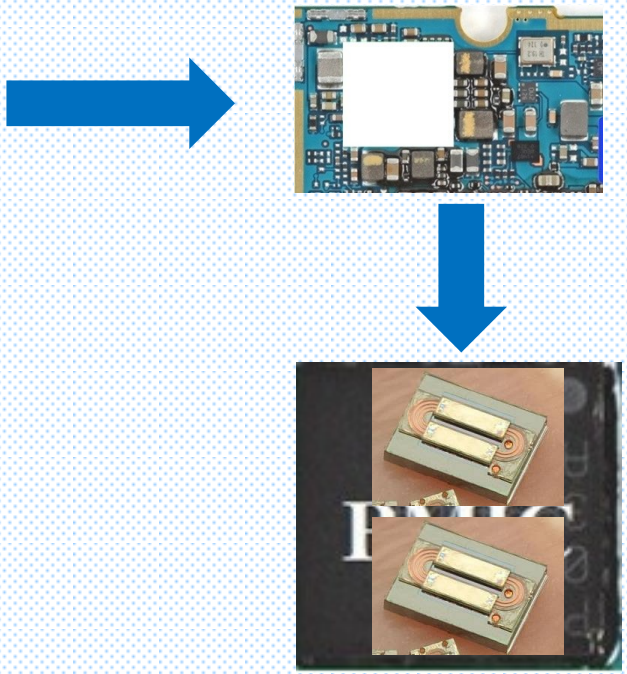


- Inductors with higher efficiency are smaller in values
  - Require the converter to operate at higher switching frequency
  - Result in significant increase in switching losses

Goal of Collaborative Research

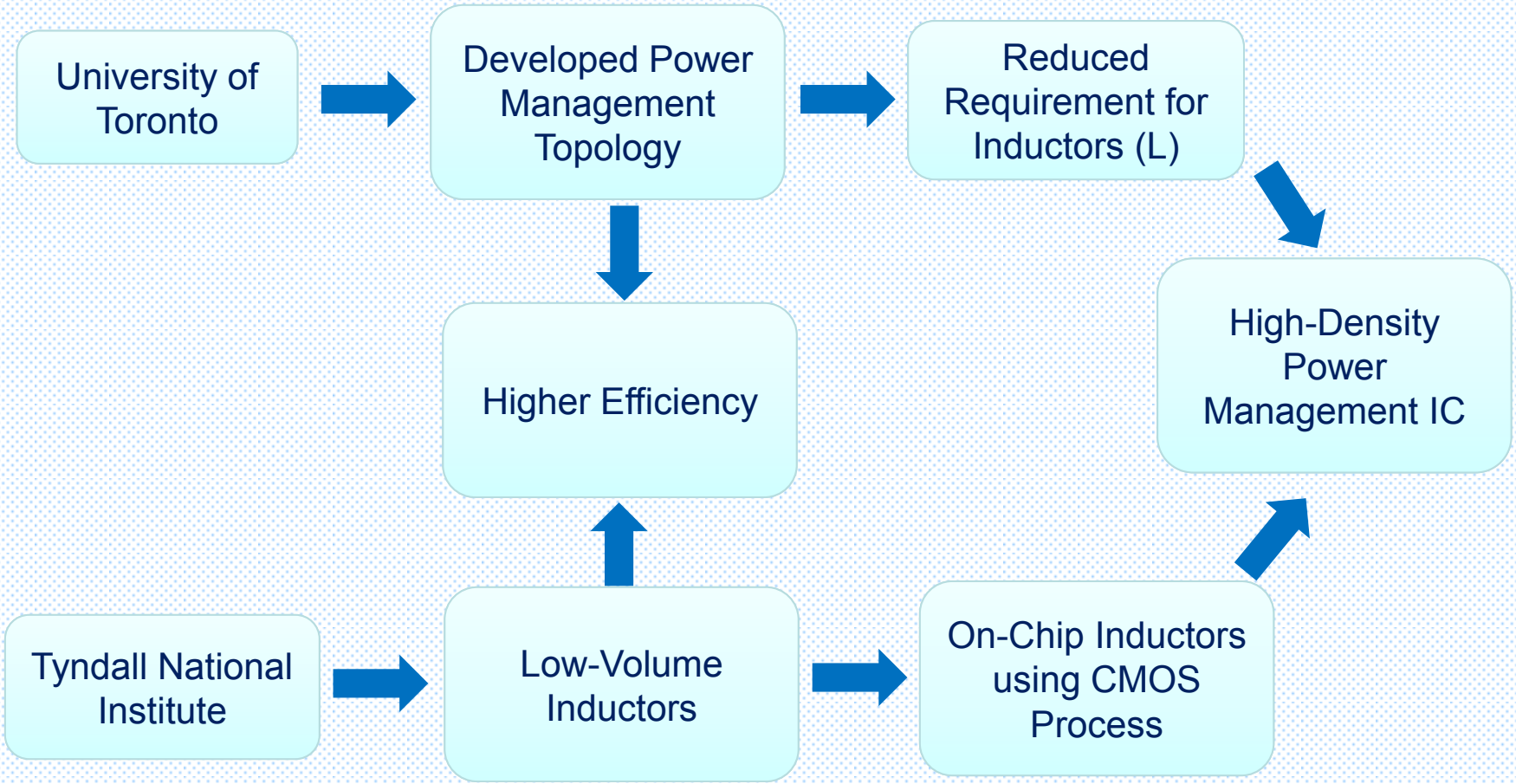
- To reduce the volume consumed by power management modules by:
  - First, developing new power management architecture
    - Reduce size of inductors
    - Increase the efficiency
  - Second, utilize advanced high efficiency on chip inductors
    - Increase power density





Goal of Collaborative Research Cont.

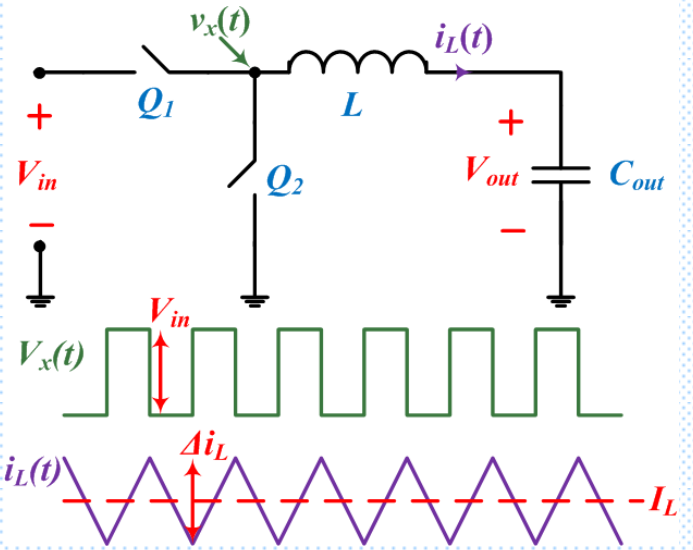
- To reduce the volume consumed by power management modules:



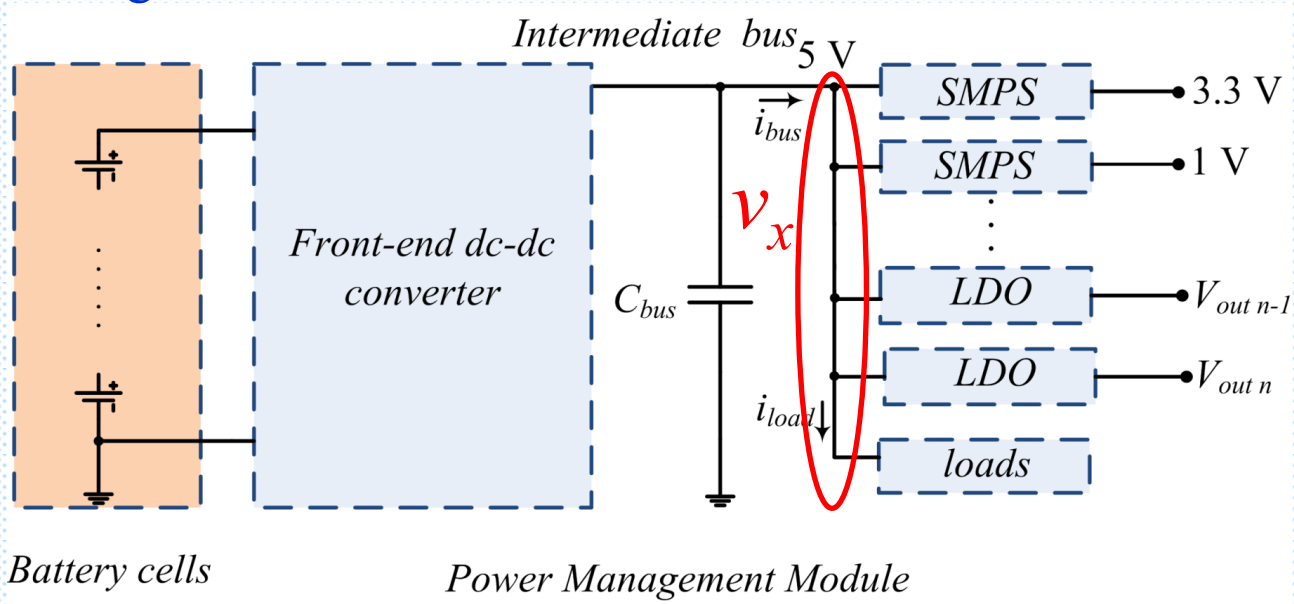
Principle of Operation

Inductor Current Ripple, $\Delta i_L = \dfrac{(V_{in} - V_{out}).D}{2.L.f_{sw}}$

Increasing switching frequency ➡ efficiency penalty



- In a conventional fixed bus voltage based architecture inductors often work with relatively high voltage swings



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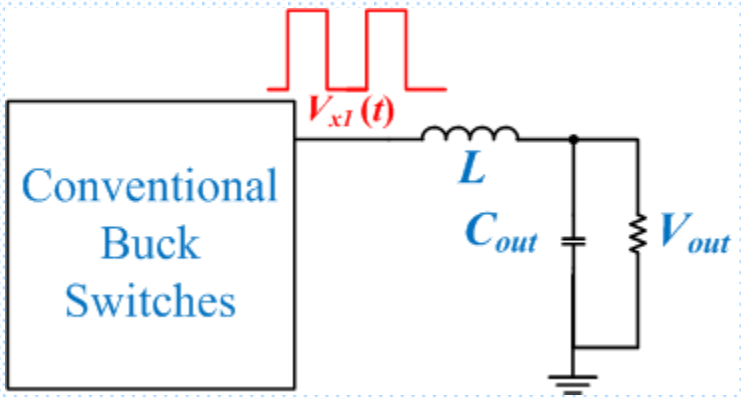
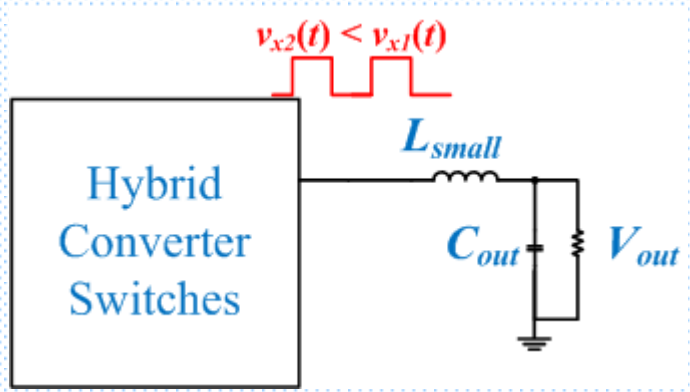


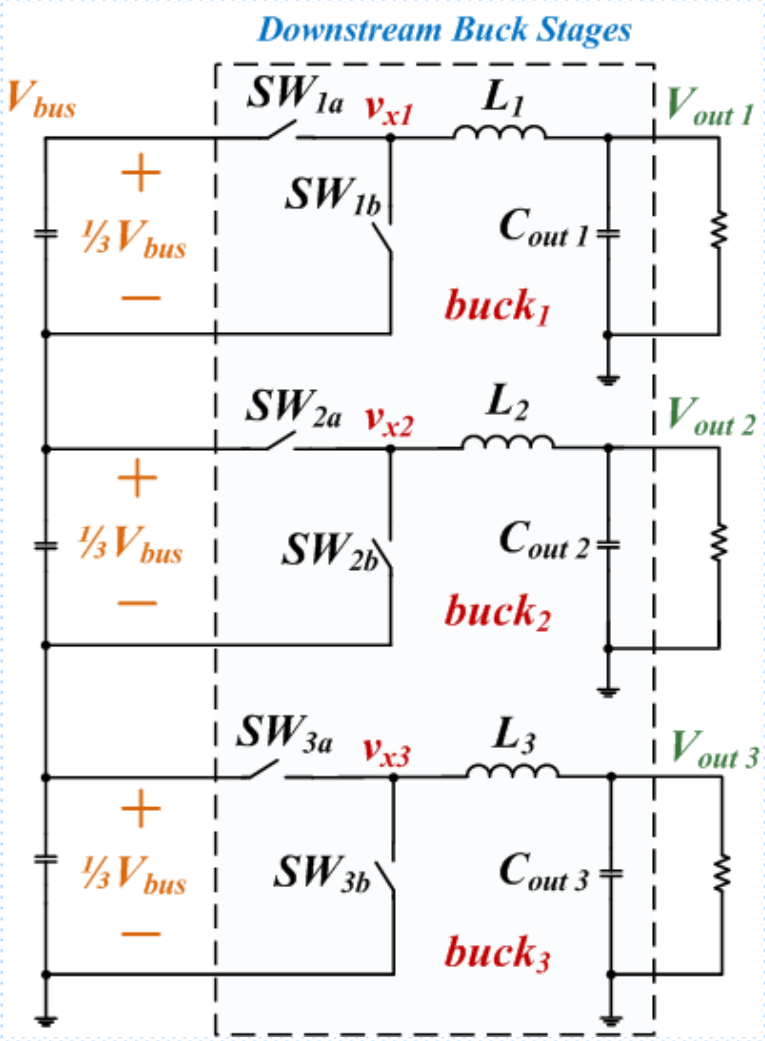


Inductor Current Ripple, $\Delta i_L = \dfrac{(V_{in} - V_{out}).D}{2.L.f_{sw}}$

- By reducing the voltage swing at the switching node, inductor sizes are reduced without:
  - Significantly increasing switching frequency
  - Paying the price in efficiency penalty
- Increased efficiency due to reduction of switching losses

Practical Implementation (APEC-2013)

- Multiple intermediate voltage levels
  - Reduced voltage swings across inductors reduce the required inductor sizes for same ripple
  - Differentially connected buck converters have increased efficiency due to reduced switching losses
  - Operating at a higher switching frequency further reduces inductor sizes

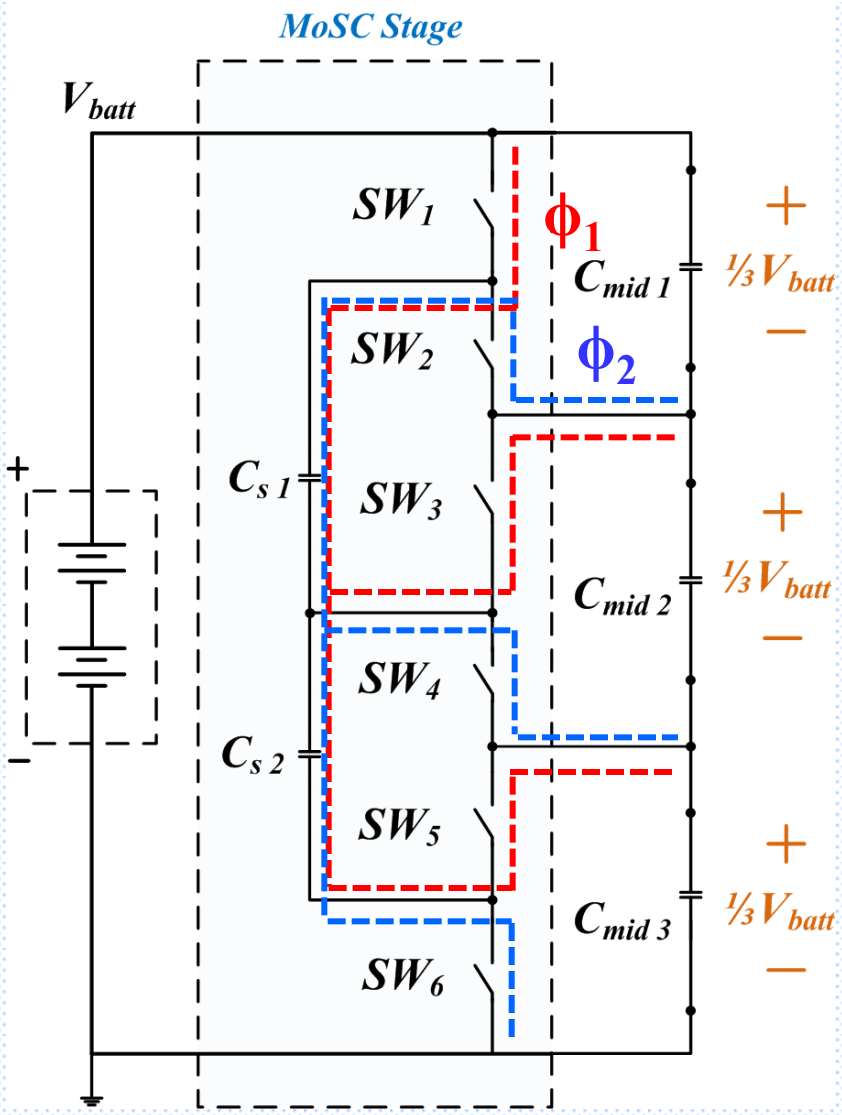


Ahsanuzzaman, S.M.; Blackman, J.; McRae, T.; Prodic, A, "A low-volume power management module for portable applications based on a multi-output switched-capacitor circuit," *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE* , pp.1473,1479, 17-21 March 2013

Practical Implementation Cont.

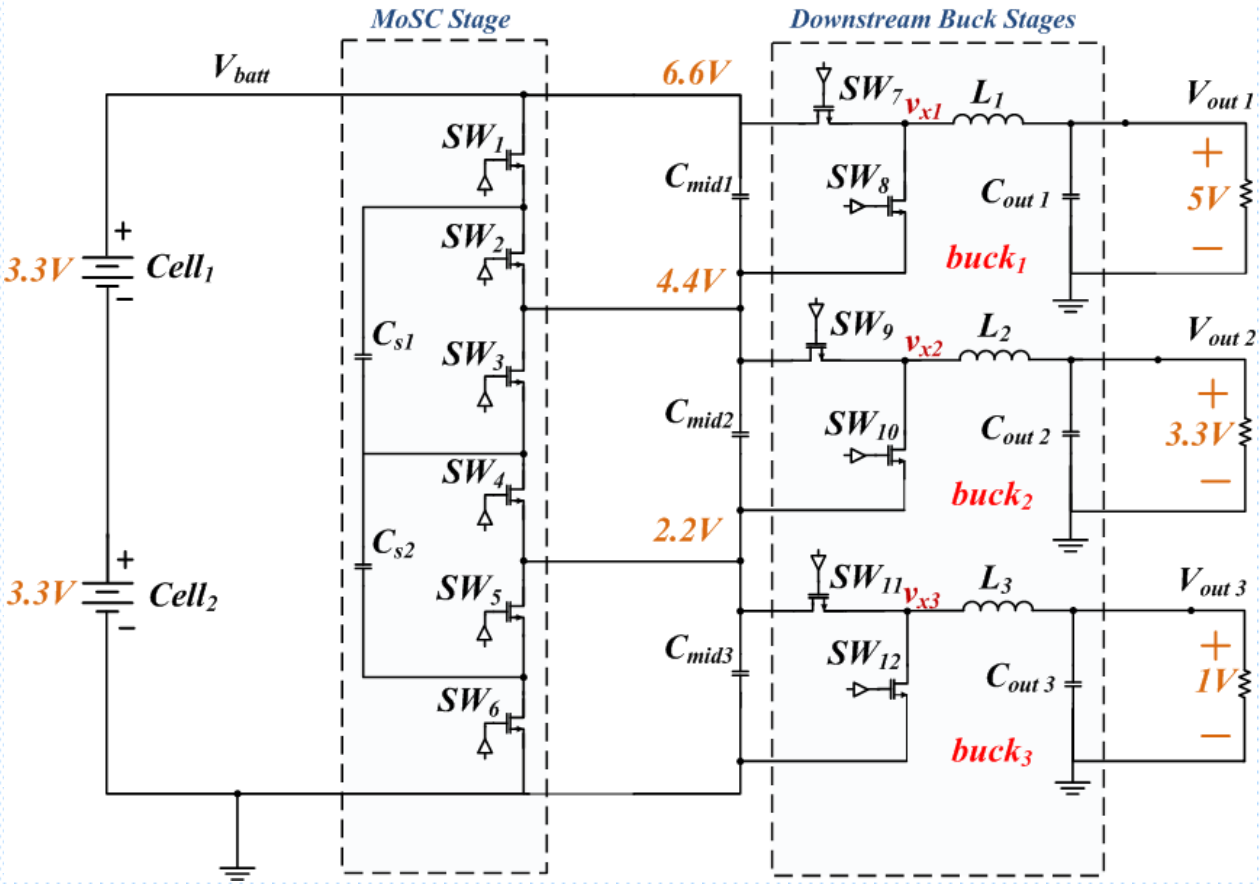
Multi-Output SC Front Stage

- Fixed-ratio switched capacitor circuits show high efficiency
- 2 flying capacitors (C_{s1} and C_{s2}) are used with 6 switches with 50% duty ratio
- Each intermediate capacitor (C_{mid1}, C_{mid2}, C_{mid3}) holds 1/3rd of the battery voltage

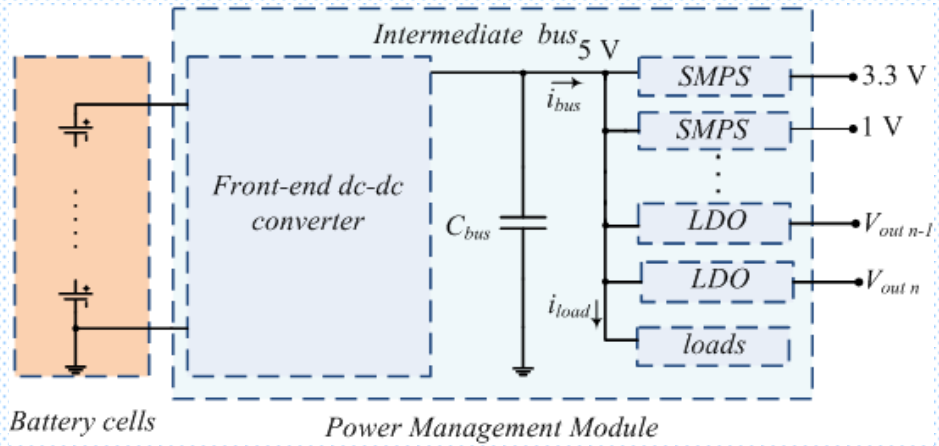


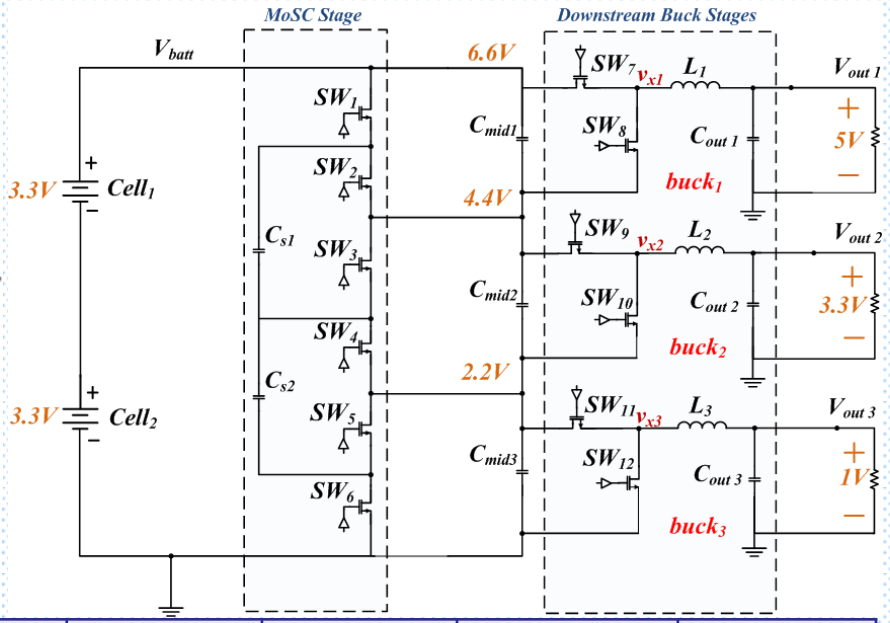
Typical Application

- 1 V output: Digital processors
- 3.3 V output: analog components (i.e. power amplifiers)
- 5 V output: USB ports and peripherals



Comparison Table



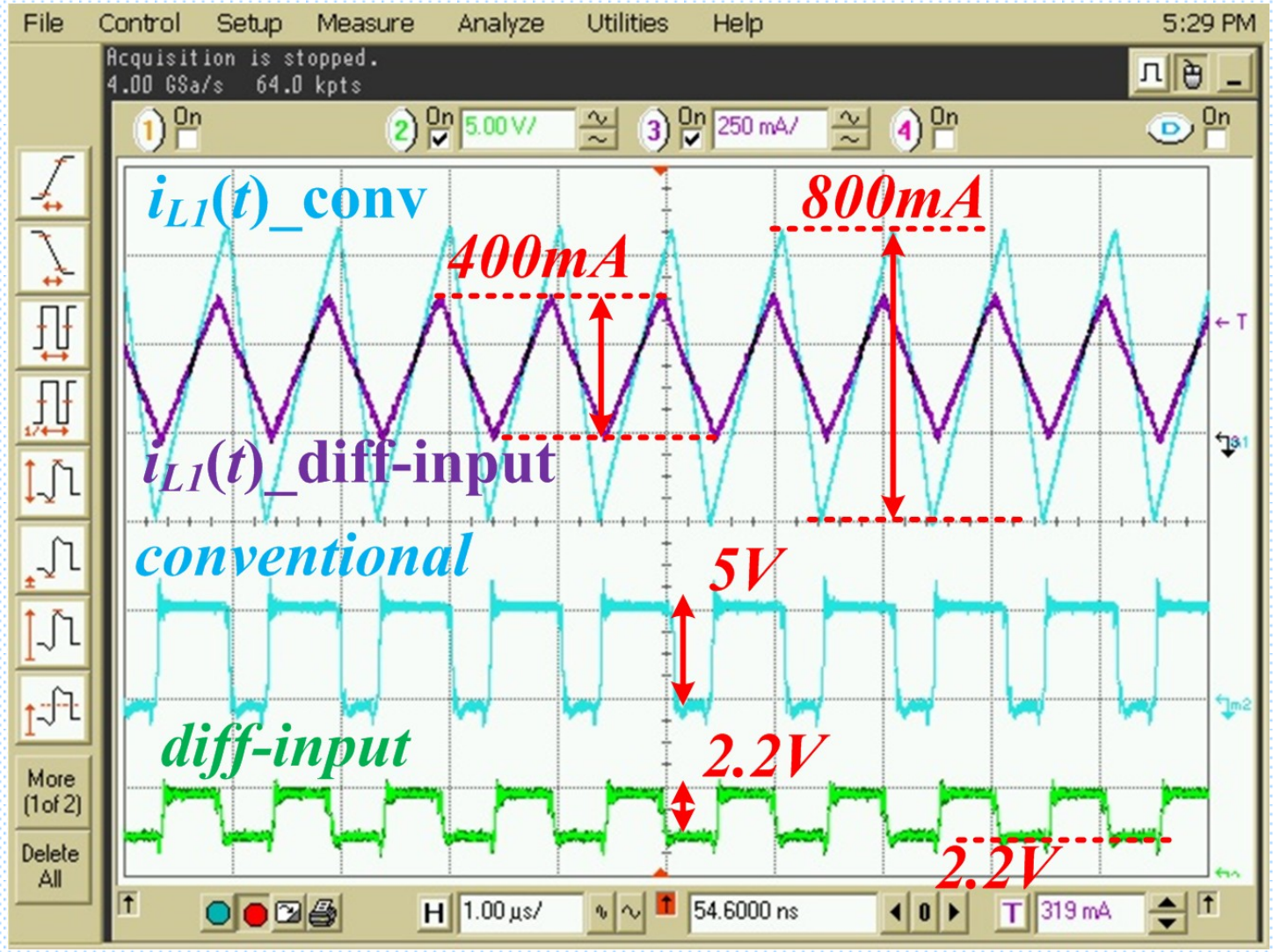


	V_{sw_norm}	$L_{\_norm}$	P_{sw_norm}	f_{sw_norm}
Diff-input buck 3.3 V	0.44	0.49	0.44	1
Diff-input buck 1 V	0.44	0.68	0.44	1
Diff-input buck 3.3 V (incr. f_{sw})	0.44	0.25	0.88	2
Diff-input buck 1 V (incr. f_{sw})	0.44	0.34	0.88	2

- Values in the table are normalized with respect to the conventional architecture (left fig)

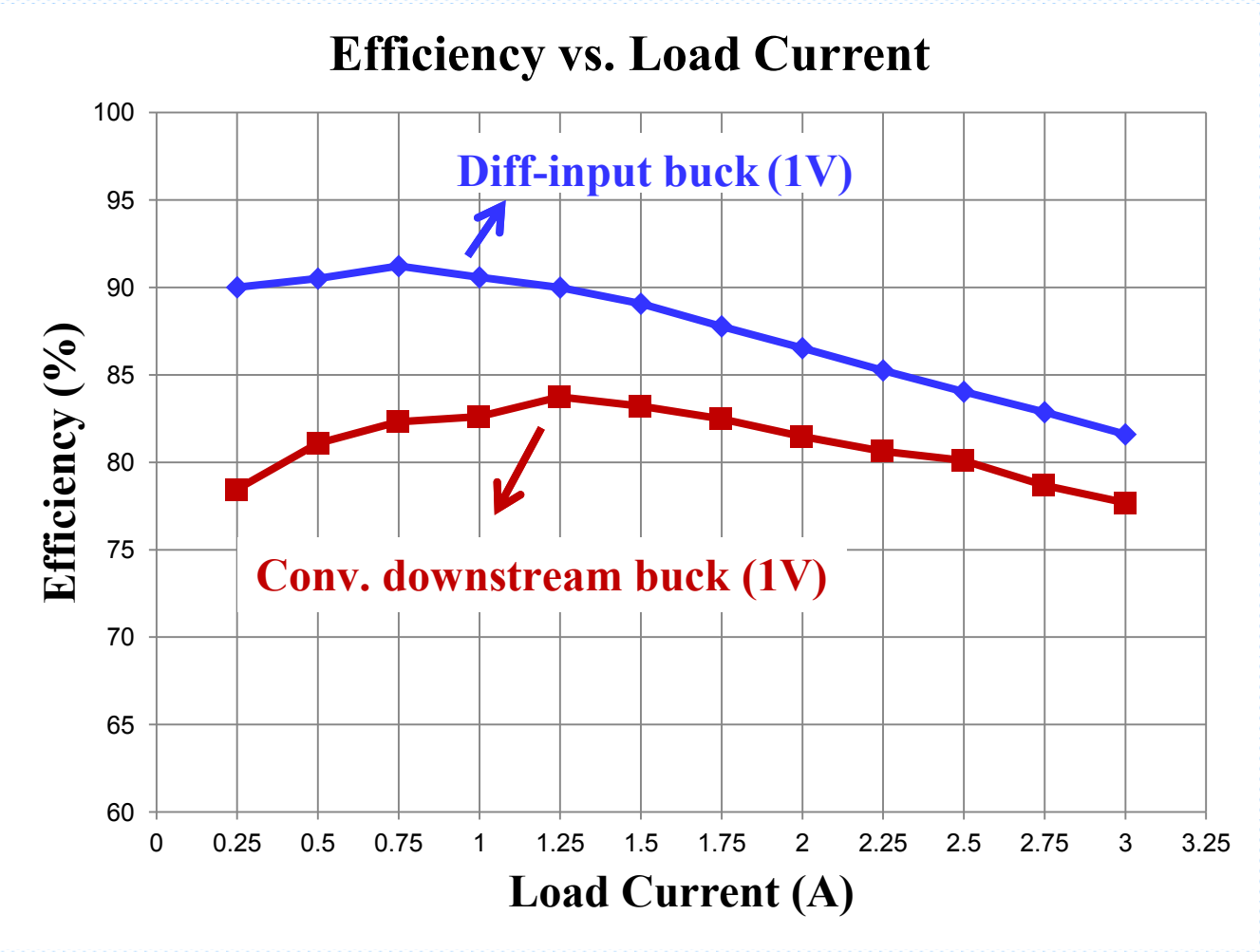
Exp. Result: Inductor Ripple Reduction

- 3.3 V buck converter: 50% ripple reduction



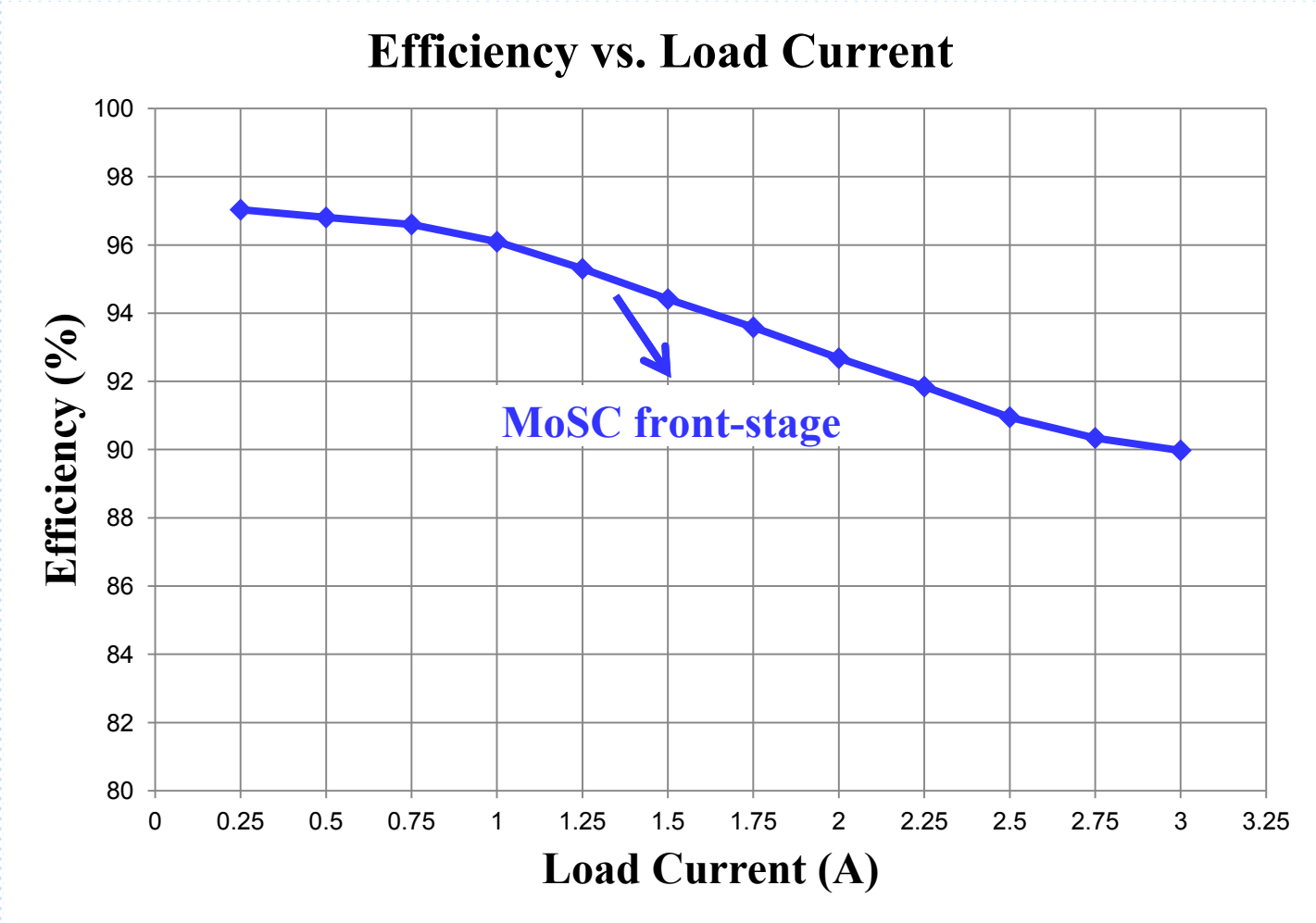
Measured Efficiency Comparison

- 1 V buck converter: 12% improvement at lighter loads



Measured System Efficiency

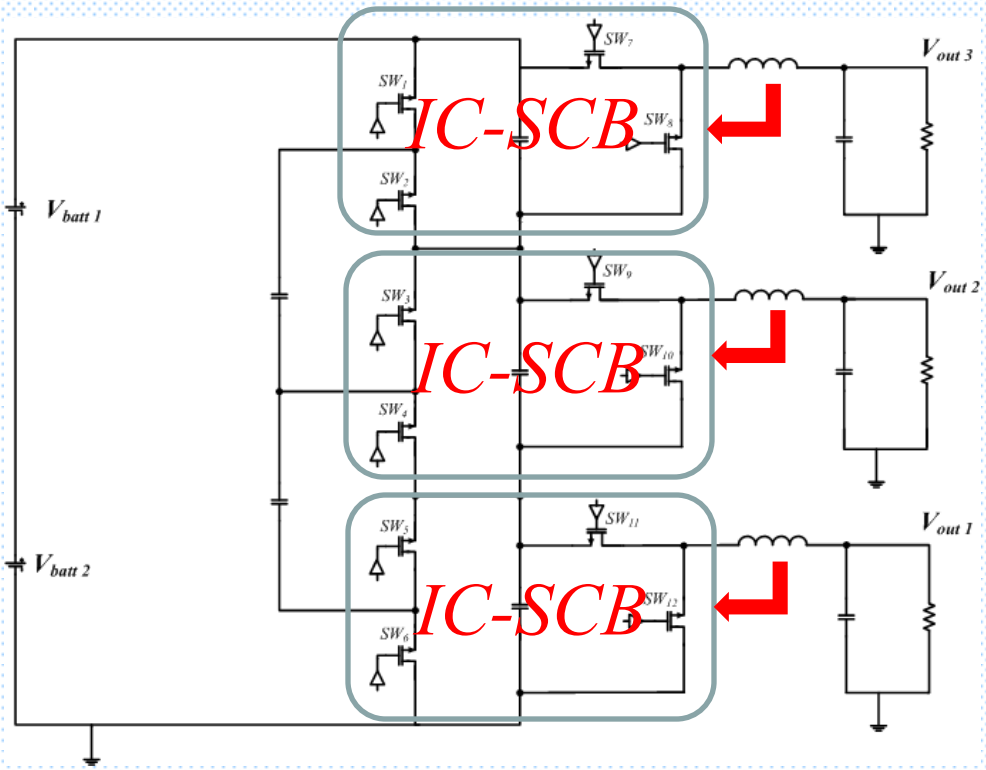
- MoSC front-end stage shows above 90% operating efficiency

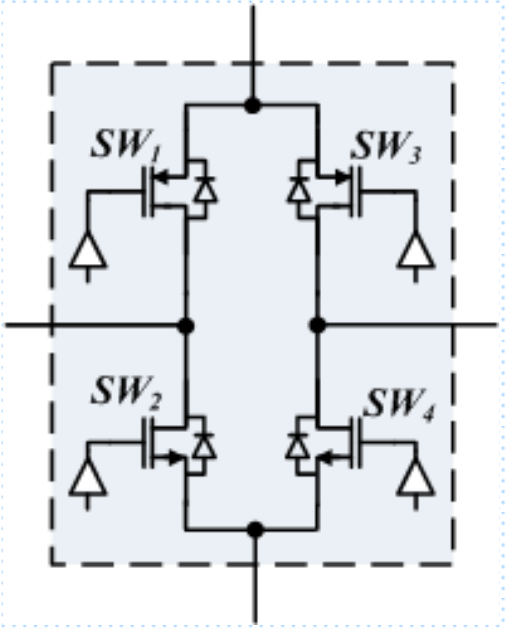


High Power Density Power Management IC Module

Design Implementation

- Introduced architecture is symmetric and hence, multi-chip implementation allows modular design
- Power stage switches with gate drivers are integrated along with mixed-signal current programmed mode (CPM) compatibility
- On-chip inductors are later packaged together to provide low-volume high density power management solution

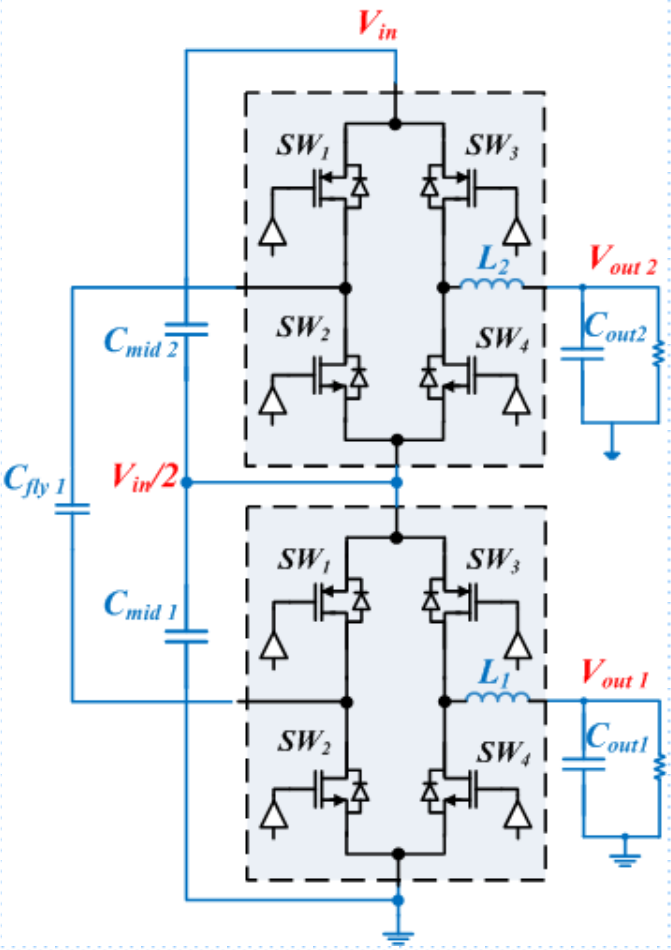




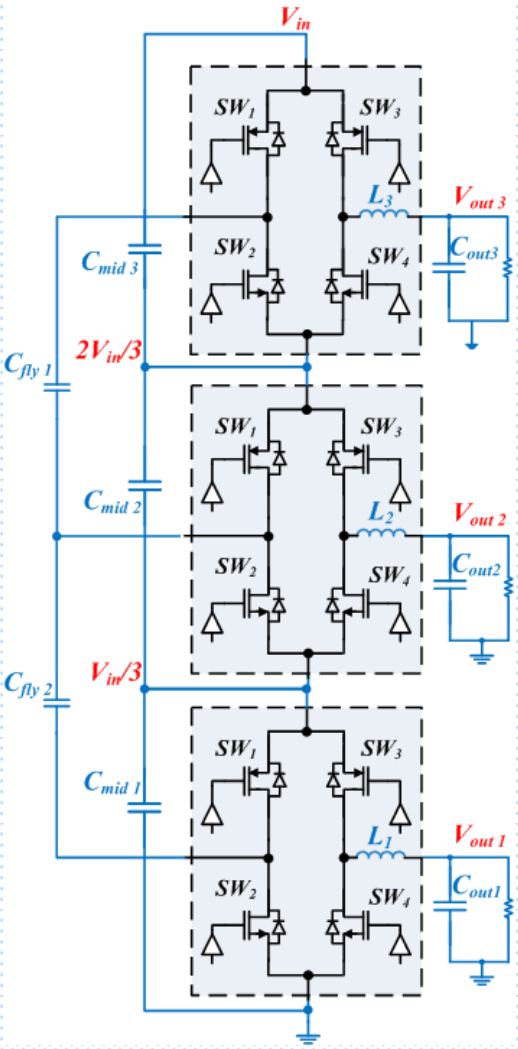
IC-Switched Cap Buck (SCB)

Design Implementation Cont.

- Designed IC can be stacked-up to provide multiple output voltages and/or to allow higher input voltages



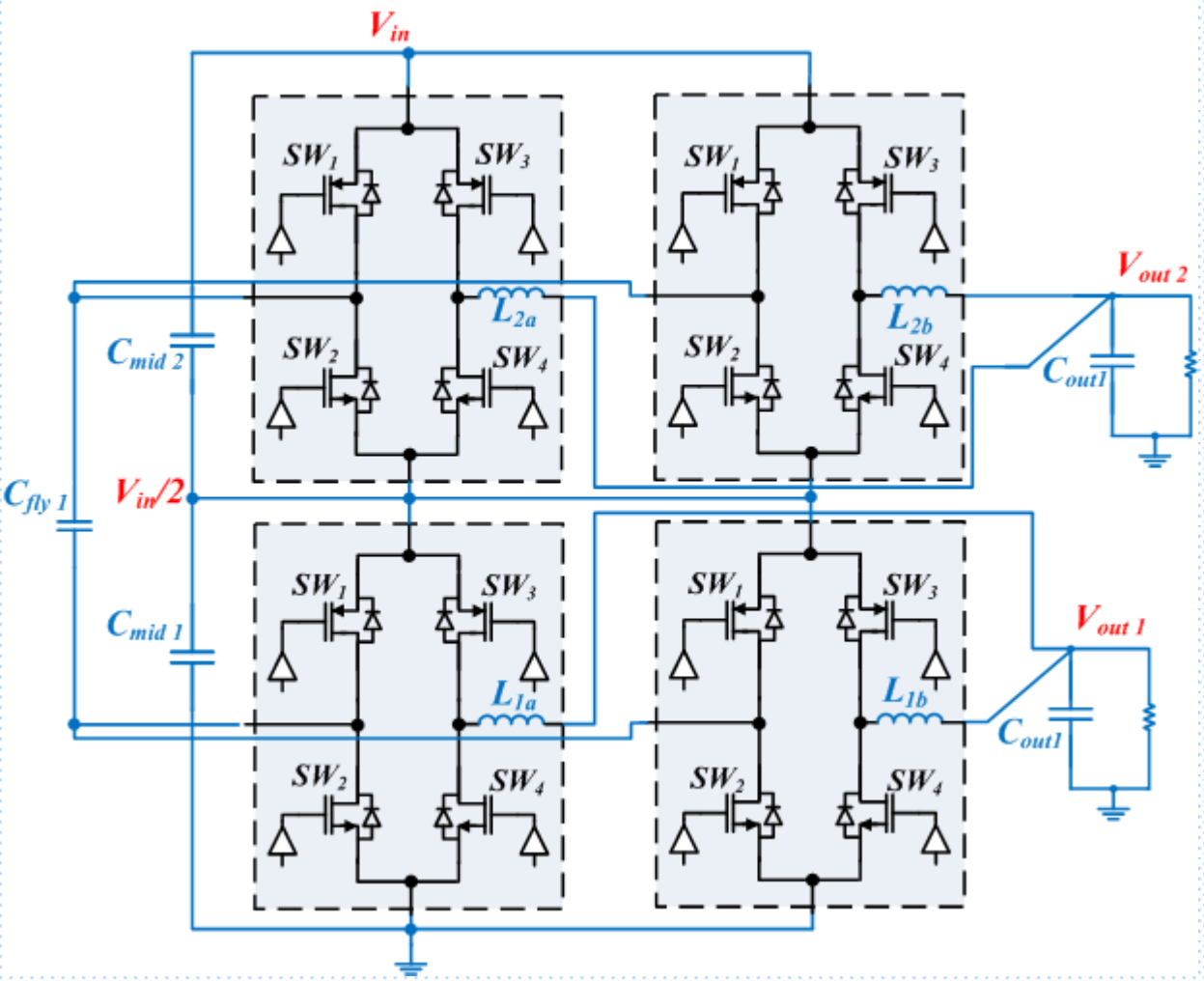
2-IC Solution



3-IC Solution

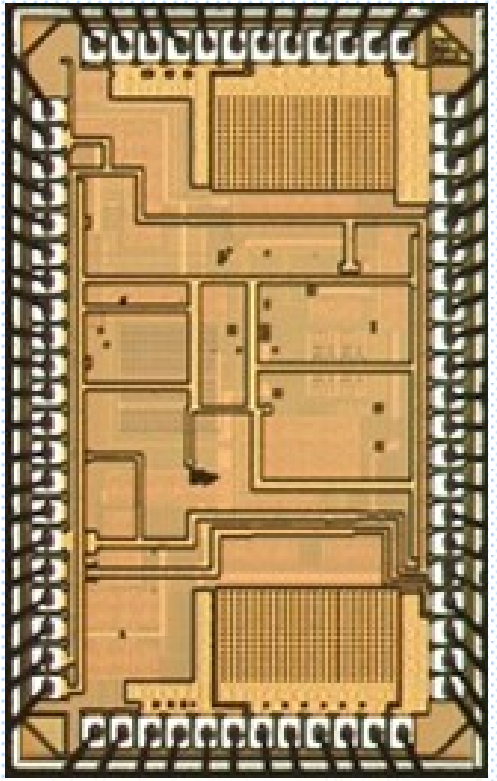
Design Implementation Cont.

- ICs can also be connected in parallel to provide higher load current.

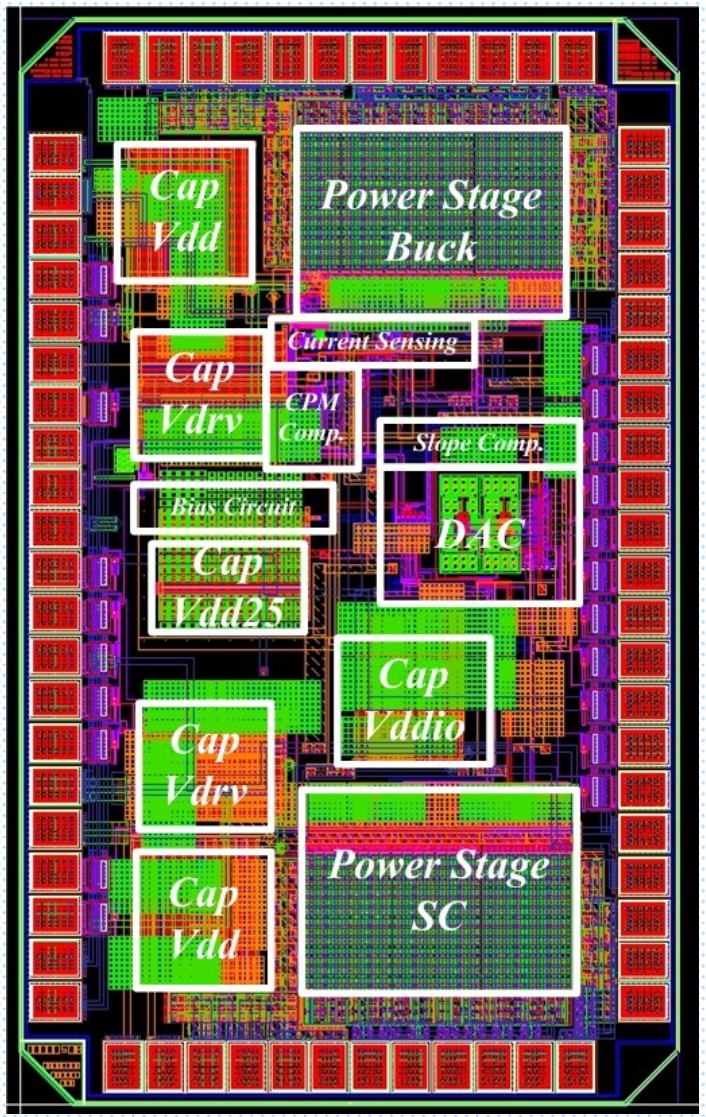


Test Chip (IC-SCB)

- Total Area: 1.5 mm X 2.5 mm
- 0.13 micron Tech.
- 1.2V FETs (thin oxide)
- 2.5V FETs (thick oxide)



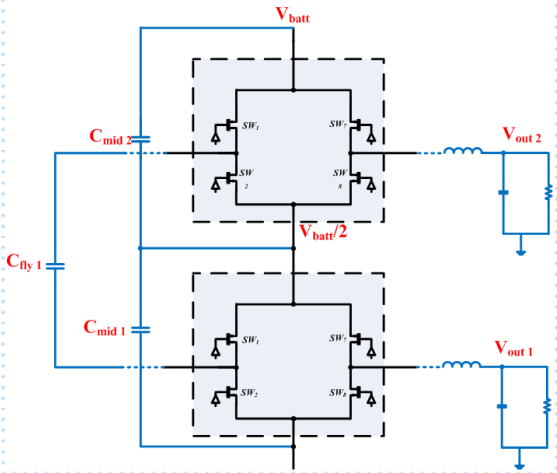
Die Photo



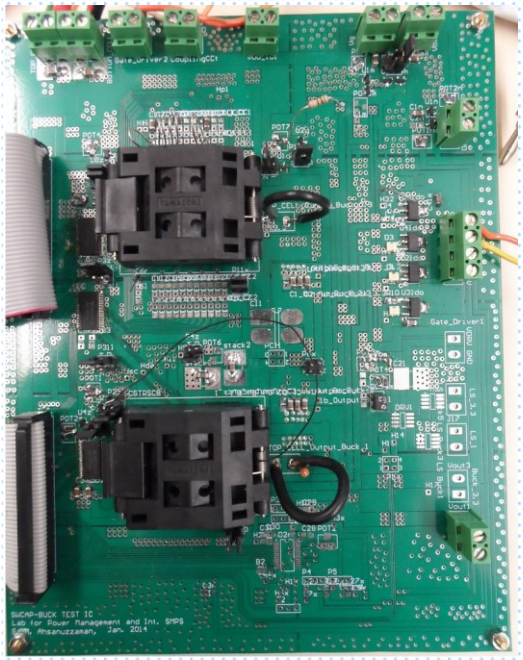
IC Layout

Experimental Setups

- 2 stacked IC-SCBs are tested for the proper system operation

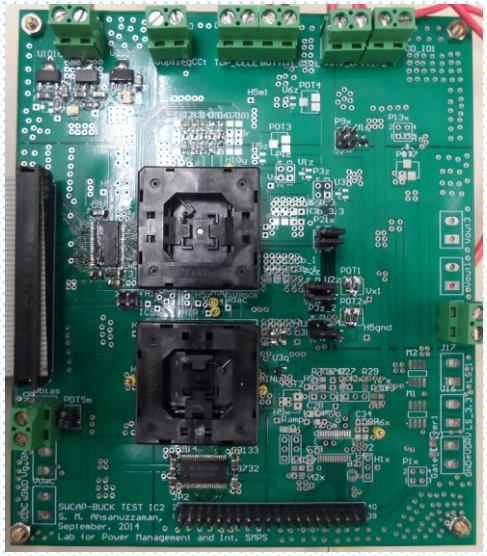


Specifications	Value	Units
f_{sw_sc}	580	KHz
f_{sw_buck}	10	MHz
V_{in}	3	V
V_{out1}, V_{out2}	1, 2.5	V
Buck L,C	100, 10	nH, µF
R_{on} *Pmos, Nmos*	150, 125	mΩ



Test Board #1

(discrete inductors)

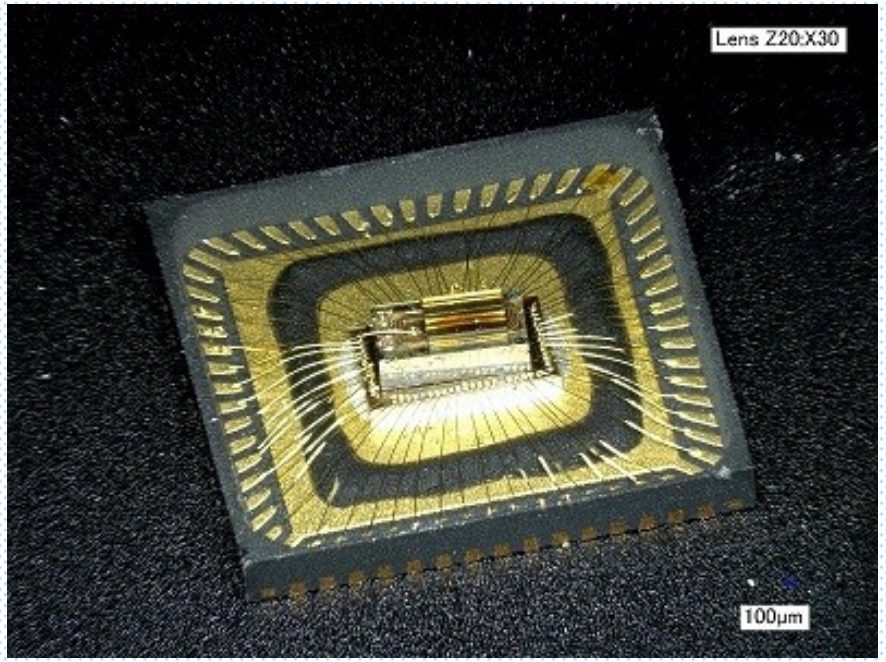


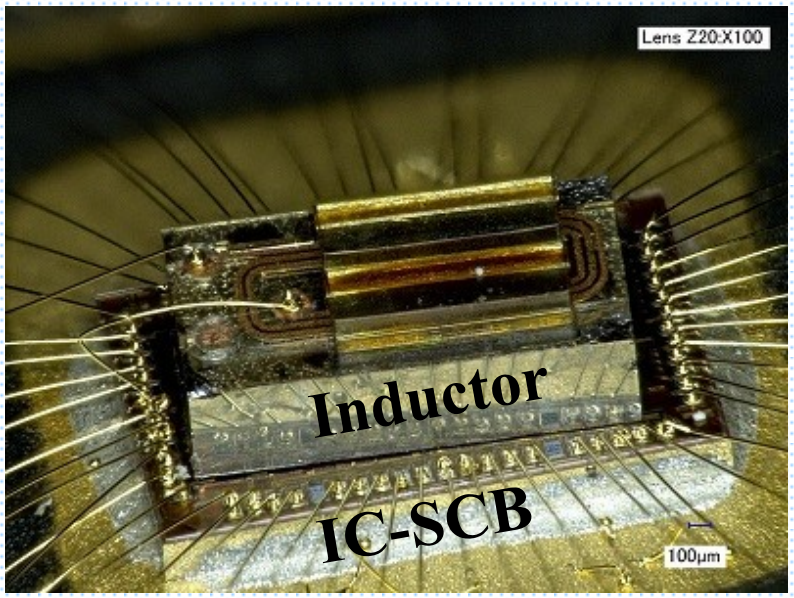
Test Board #2

(on-chip inductors)

IC Packaging with Inductors

- Bonding picture: 1-IC
  - Inductor (0603) is placed on top of the IC (1.5mm X 2.5mm)
  - 60 QFN Package: 7mm X 7mm



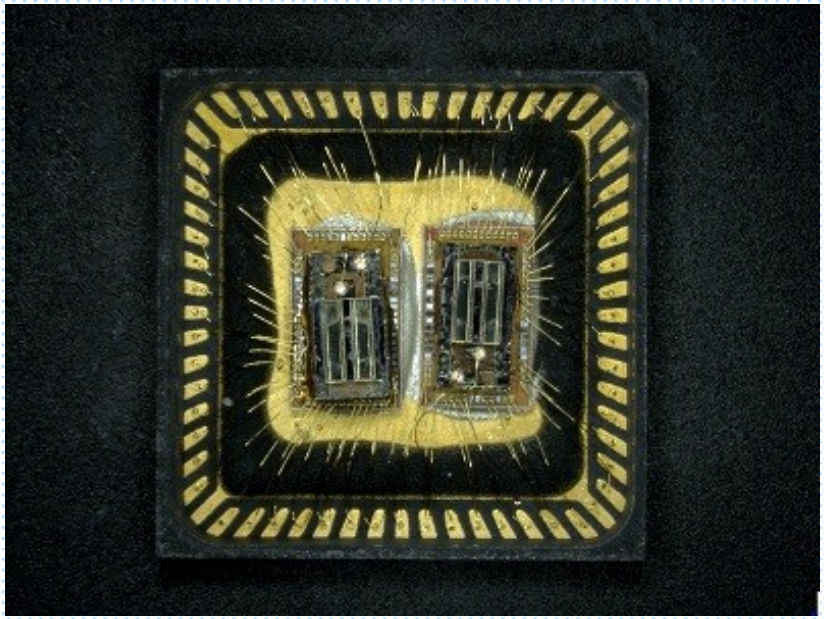


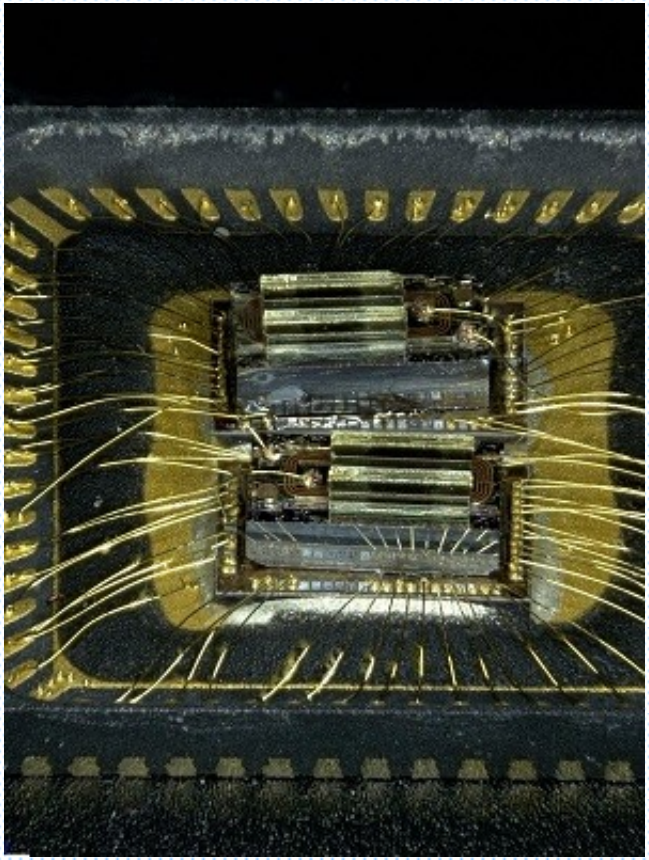
Zoomed

Size	Frequency	Target Inductance	Turn number	Width	Length	Core length	Rdc	Eff.
"0603" --2	25 MHz	130 nH	4	686	1728	1150	0.269	89.65

IC Packaging with Inductors

- Bonding picture: 2-ICs
  - Inductors (0603) are placed on top of the ICs (1.5mm X 2.5mm)
  - 60 QFN Package: 7mm X 7mm





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Size	Frequency	Target Inductance	Turn number	Width	Length	Core length	Rdc	Eff.
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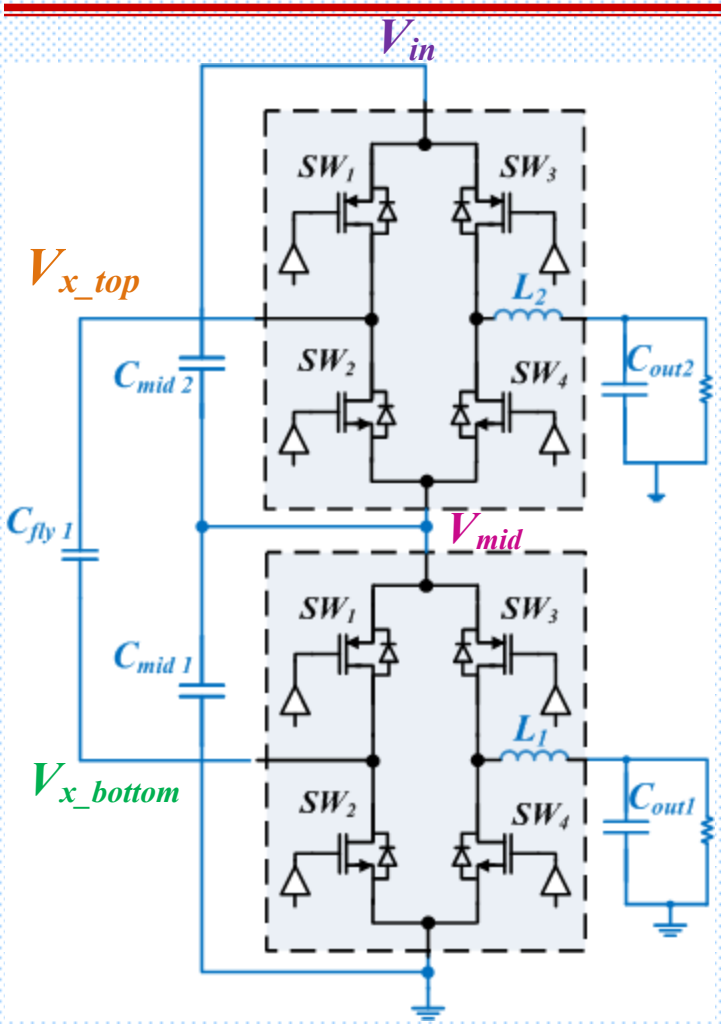
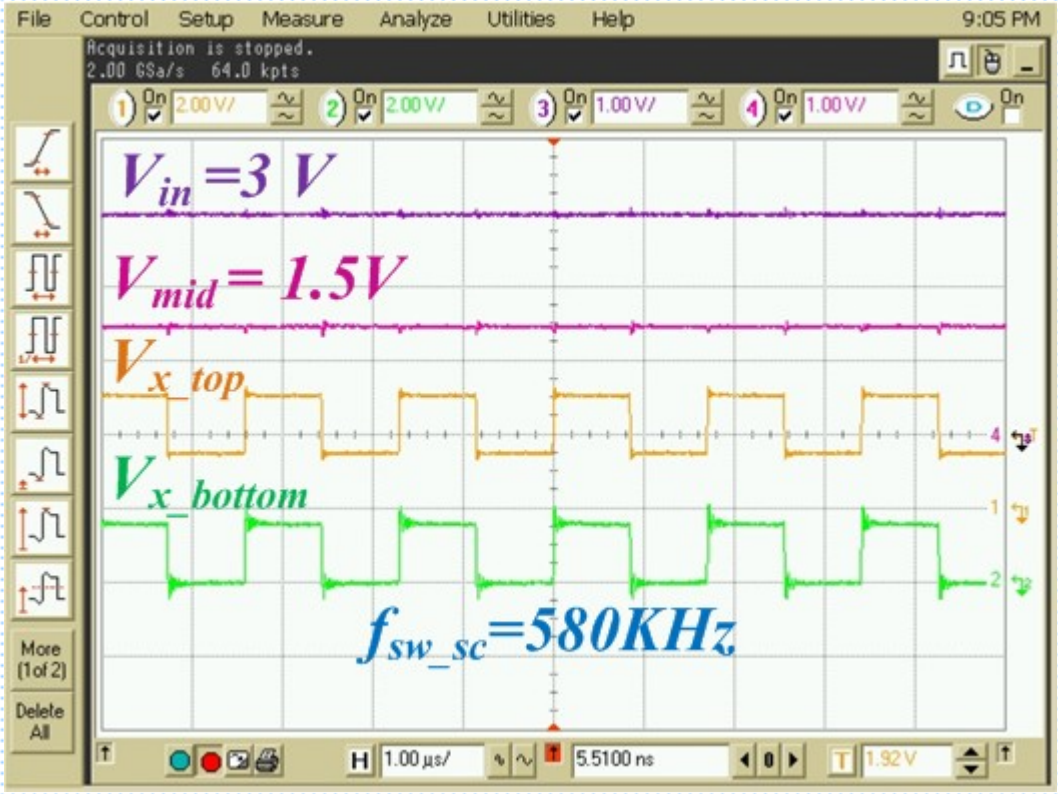
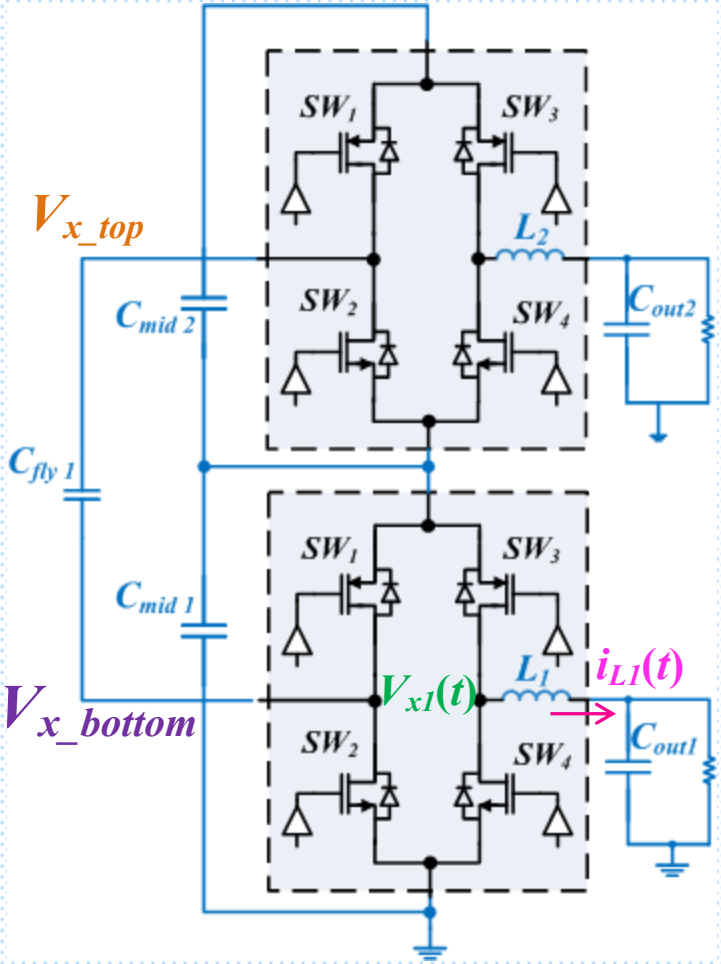
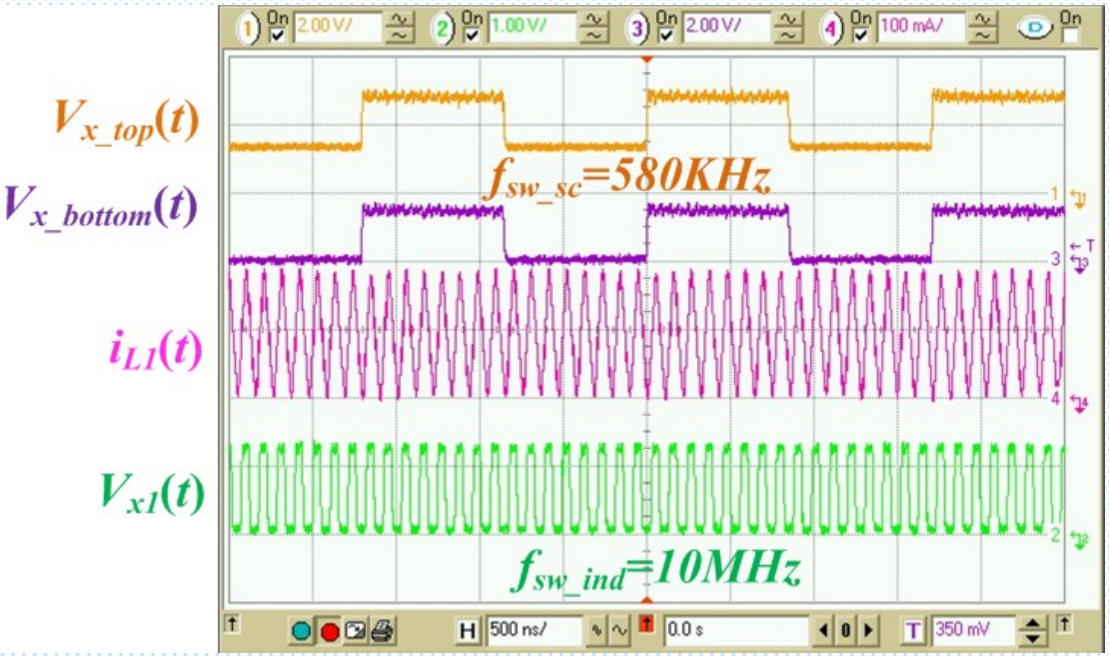
Experimental Results Cont.



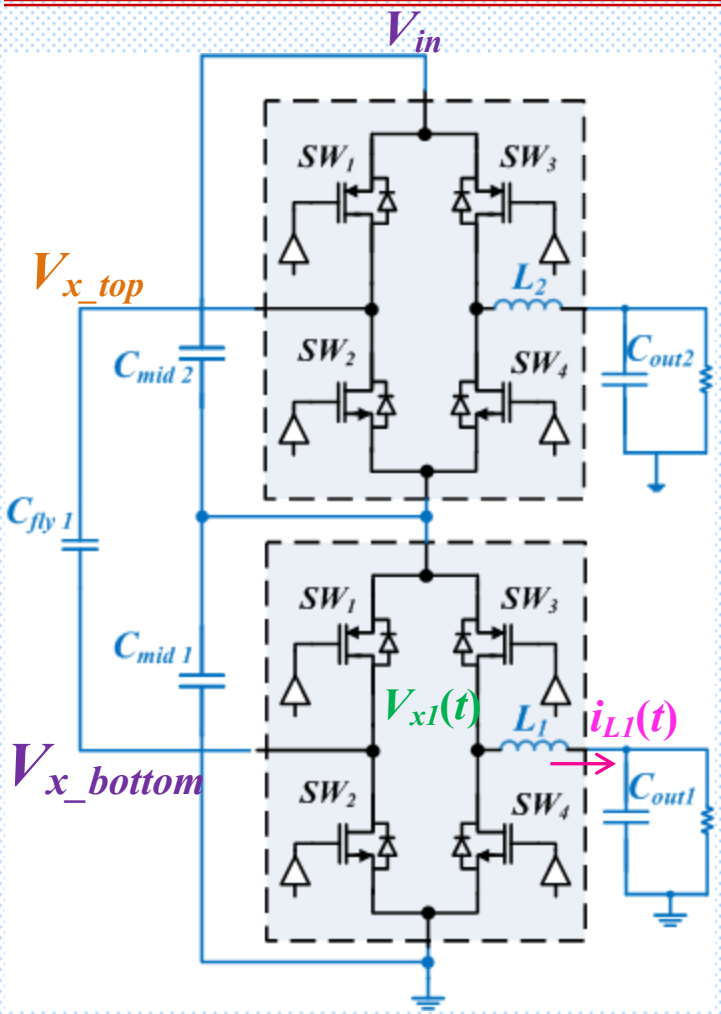


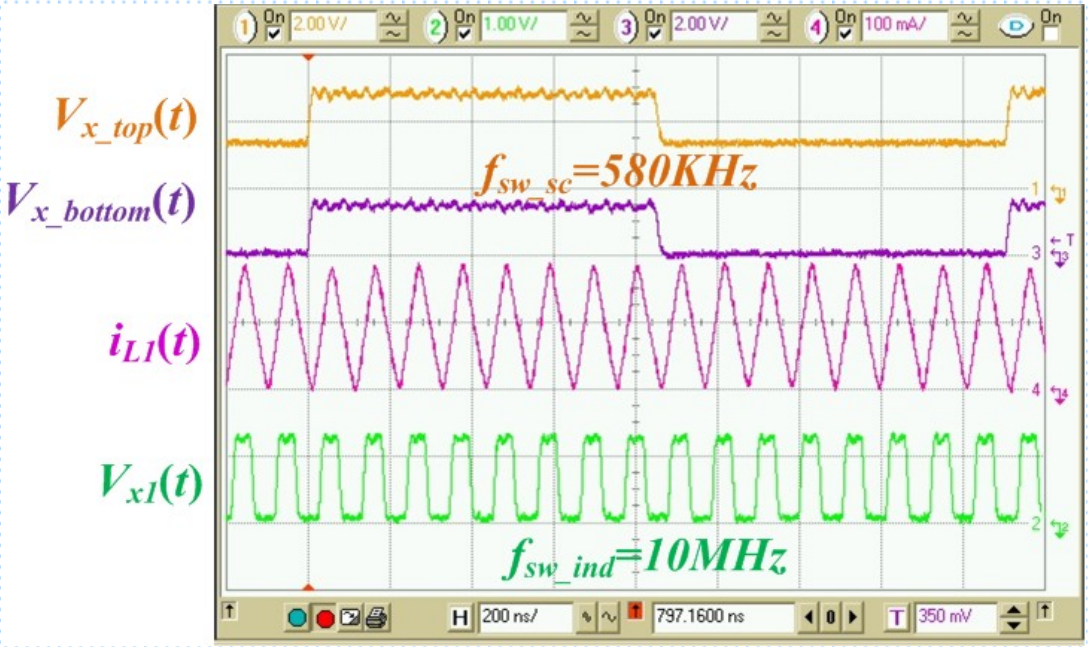
Experimental Results Cont.





Experimental Results Cont.





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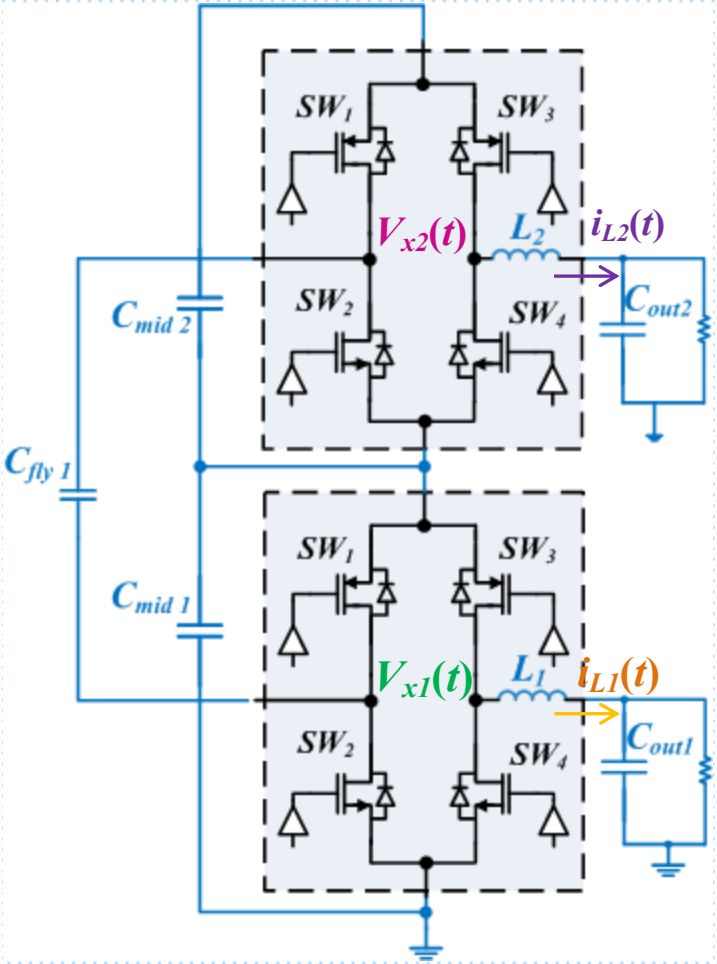

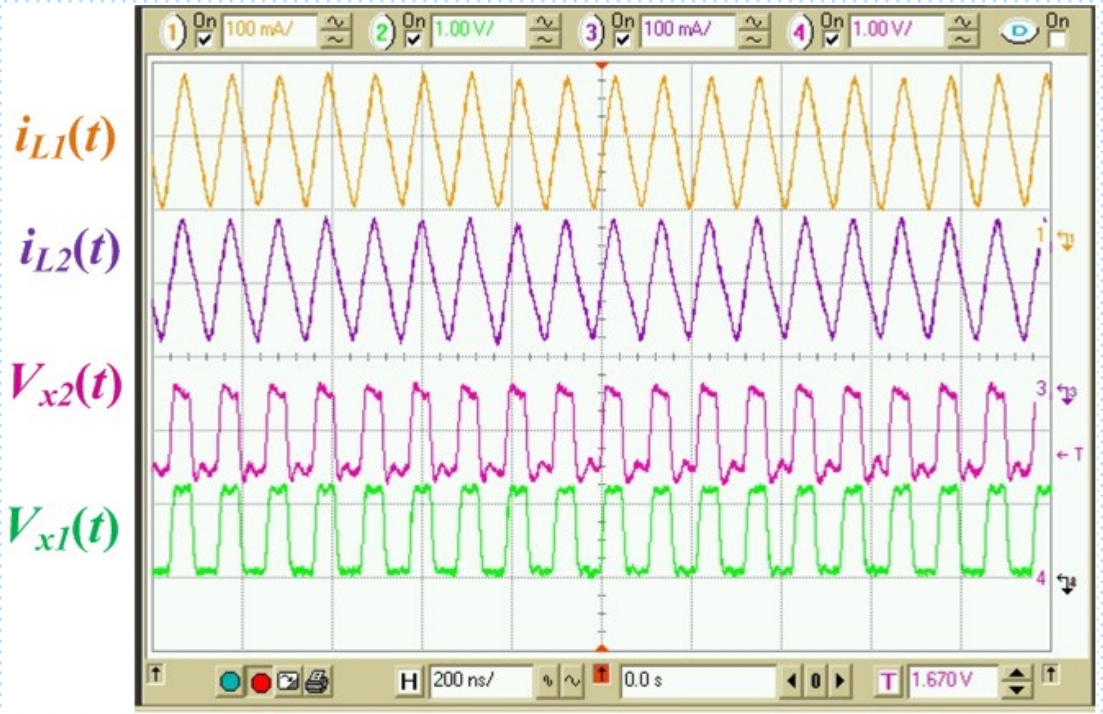

Conclusions

- Introduced a high power density hybrid power management IC where:
  - SC voltage divider allows reducing voltage swings at the switching nodes of the inductor based differentially-connected stages
  - Reduces inductor volume without the need for significantly increasing switching frequency
  - Modular design allows easy adoption for multiple applications
  - Packaging the silicon dies with inductors shows an increased level of on-chip integration of the power management architectures
  - Future work will be focused on designing PMICs with on-chip inductors on the same die

Acknowledgement

The authors would like to acknowledge **Giovanni Garcea** and **Francesco Carobolante** from **Qualcomm Inc.** for their support and advice throughout the development of the power management modules.

We would also like to acknowledge **Ken Rodgers** and **Finbarr Waldron** from Packaging Group - **Tyndall** National Institute for package assembly and **Enterprise Ireland** for funding the inductor development.

Thank You